WHAT IS CLAIMED IS:

1. A modulator using a delta-sigma conversion method, and comprising:

component separating unit separating a signal component and an error component of an input signal from each other;

delta-sigma modulator modulating the error component separated by said component separating unit; and

output operating unit operating the signal component separated by said component separating unit and the error component modulated by said delta-sigma modulator.

2. The modulator according to claim 1, wherein

said component separating unit includes a first quantizer quantizing a digital input signal, and

an adder adding said digital input signal to said signal component provided from said first quantizer.

3. The modulator according to claim 2, wherein

said delta-sigma modulator includes:

a plurality of integrators,

a second quantizer quantizing an output of the integrator in the final stage, and

a delay element delaying an output of said second quantizer to perform negative feedback by sending the delayed output to said plurality of integrators.

4. The modulator according to claim 2, wherein

said delta-sigma modulator includes a plurality of single-stage delta-sigma modulators each including:

a plurality of integrators,

a second quantizer quantizing an output of the integrator in the final stage, and

a delay element delaying an output of said second quantizer, and performing negative feedback by sending the delayed output to said plurality of integrators; and

said plurality of single-stage delta-sigma modulators are cascaded.

5. The modulator according to claim 2, further comprising:

an attenuator connected between said adder and said delta-sigma modulator, and having a coefficient smaller than one.

6. The modulator according to claim 1, wherein

said component separating unit includes:

a multibit quantizer quantizing a digital input signal to provide a multibit form, and

an adder adding said digital input signal to said signal component provided from said multibit quantizer.

7. The modulator according to claim 1, wherein

said component separating unit includes:

a first quantizer quantizing an analog input signal,

a first digital-to-analog converter converting said signal component provided from said first quantizer to an analog signal, and

an adder adding said analog input signal to said analog signal provided from said first digital-to-analog converter.

8. The modulator according to claim 7, wherein

said delta-sigma modulator includes:

a plurality of integrators,

a second quantizer quantizing an output of the integrator in the final stage,

a second digital-to-analog converter converting an output of said second quantizer to an analog signal, and

a delay element delaying the analog signal provided from said second digital-to-analog converter, and performing negative feedback by sending

the delayed analog signal to said plurality of integrators.

9. The modulator according to claim 7, wherein

said delta-sigma modulator includes a plurality of single-stage delta-sigma modulators each including:

a plurality of integrators,

a second quantizer quantizing an output of the integrator in the final stage,

a second digital-to-analog converter converting an output of said second quantizer to an analog signal, and

a delay element delaying the analog signal provided from said second digital-to-analog converter, and performing negative feedback by sending the delayed analog signal to said plurality of integrators; and

said plurality of single-stage delta-sigma modulators are cascaded.

10. The modulator according to claim 7, further comprising:

an attenuator connected between said adder and said delta-sigma modulator, and having a coefficient smaller than one.

11. The modulator according to claim 1, wherein

said component separating unit includes:

a multibit quantizer quantizing an analog input signal to provide a multibit form,

a digital-to-analog converter converting said signal component provided from said multibit quantizer to an analog signal, and

an adder adding said analog input signal to the analog signal provided from said digital-to-analog converter.